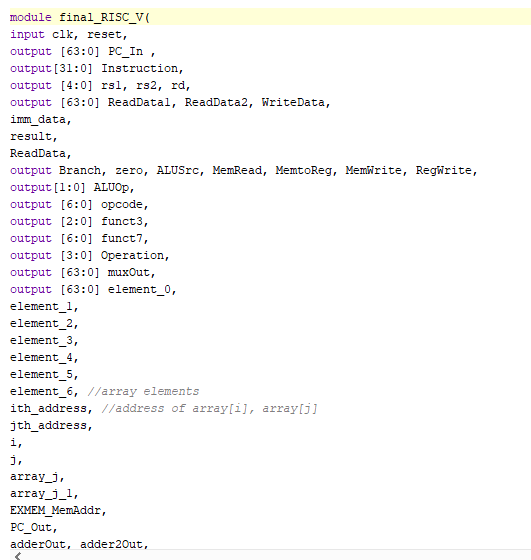
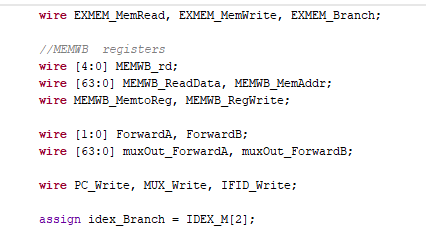
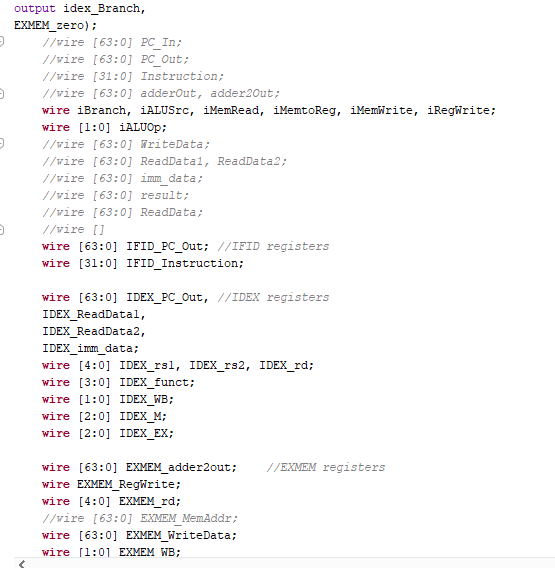
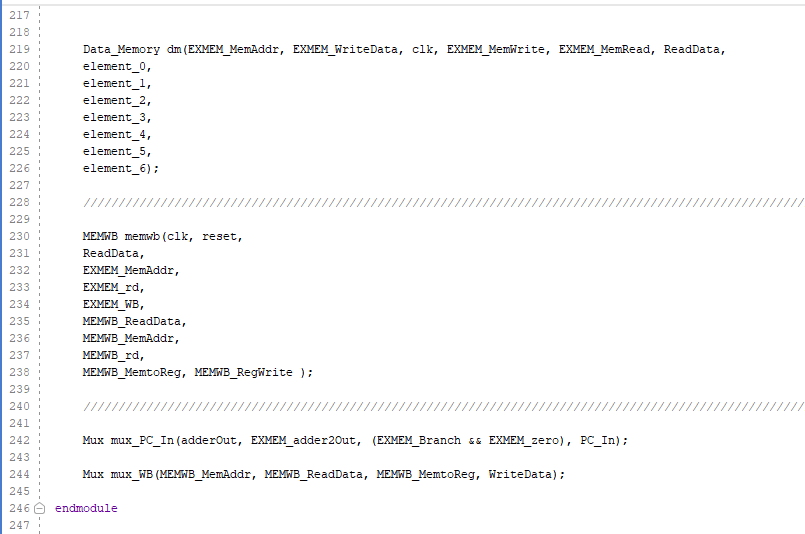
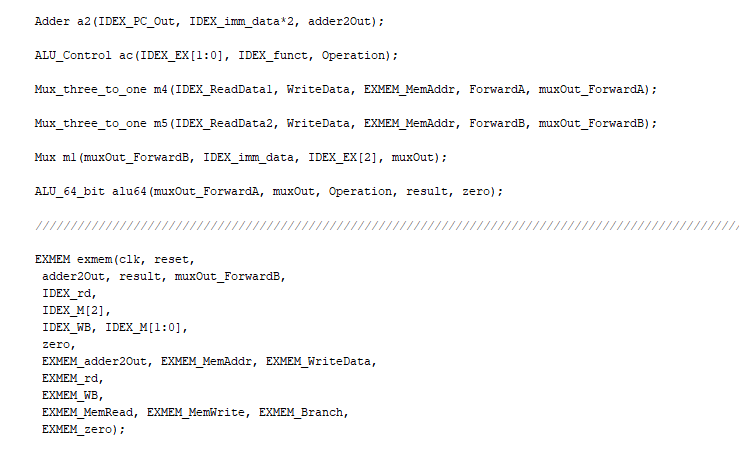
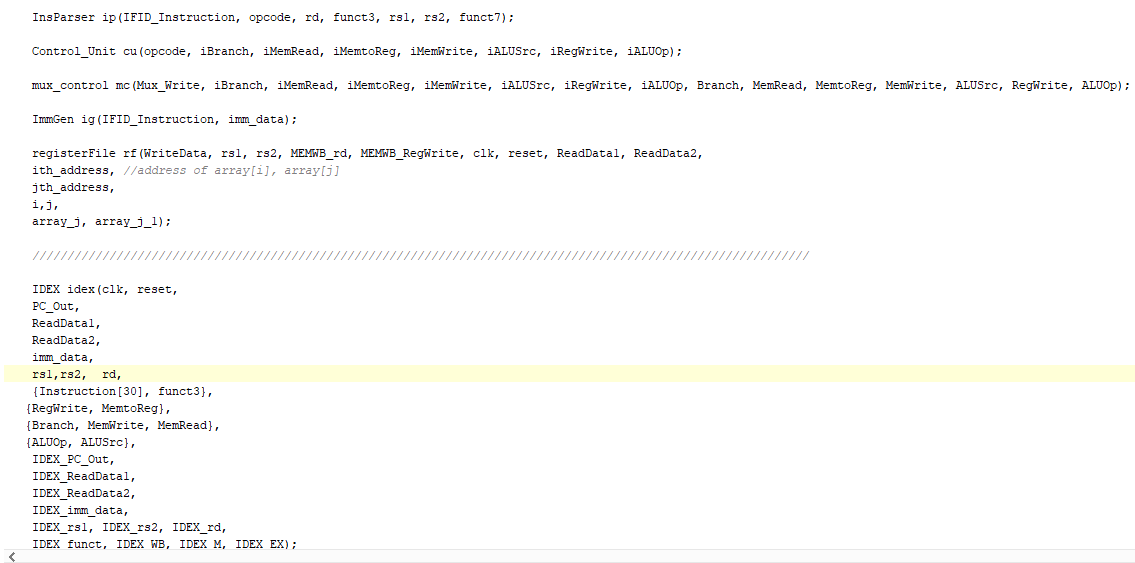
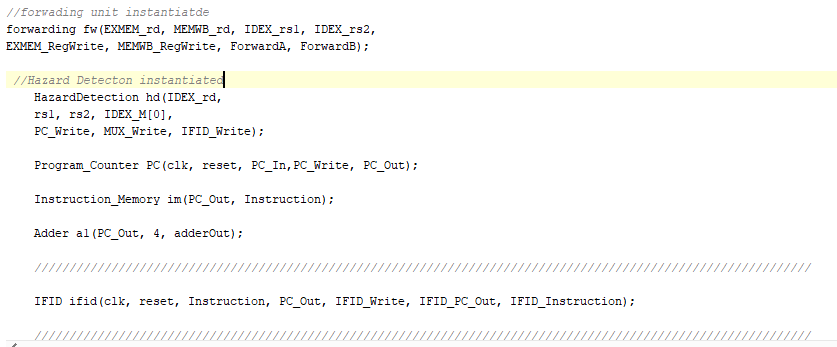
**Pipelined RISC V Processor**

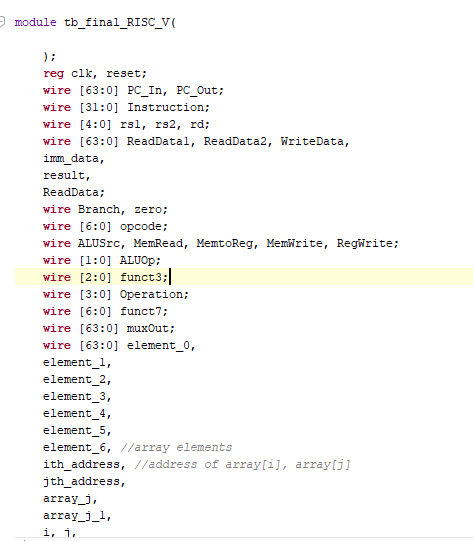
**Top Module**

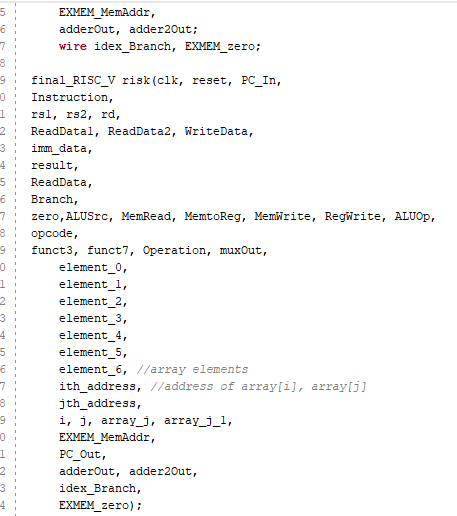
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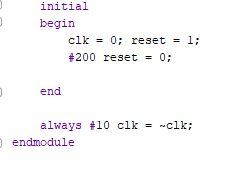
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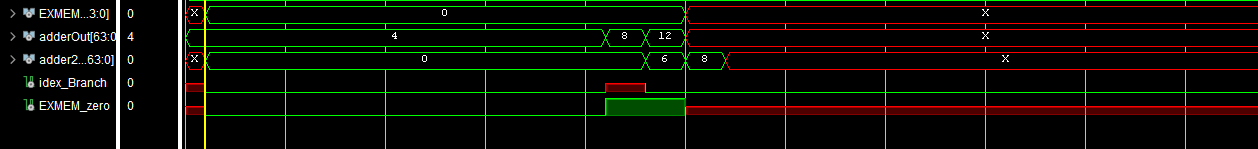
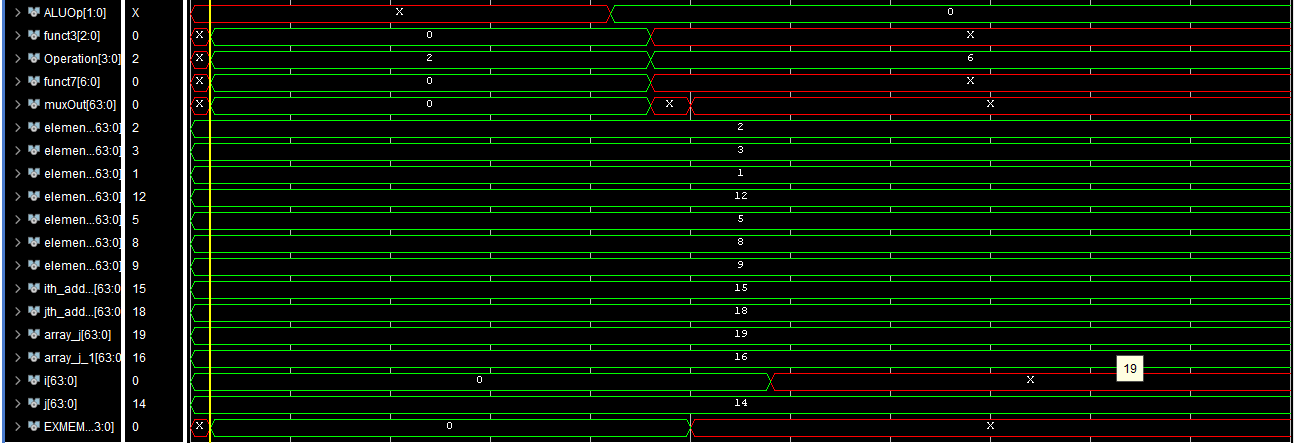
**TestBench**

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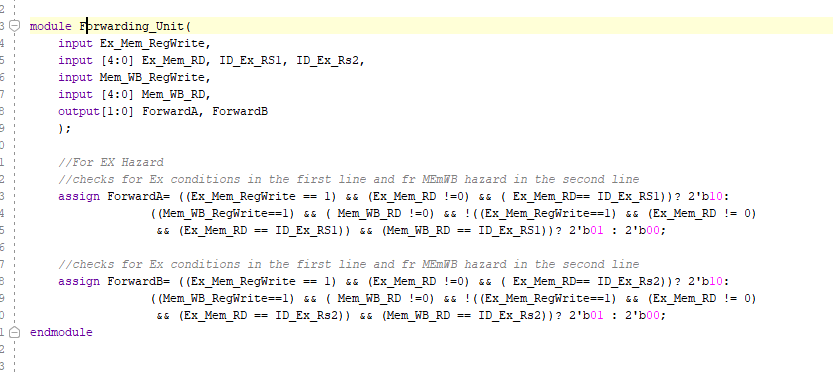
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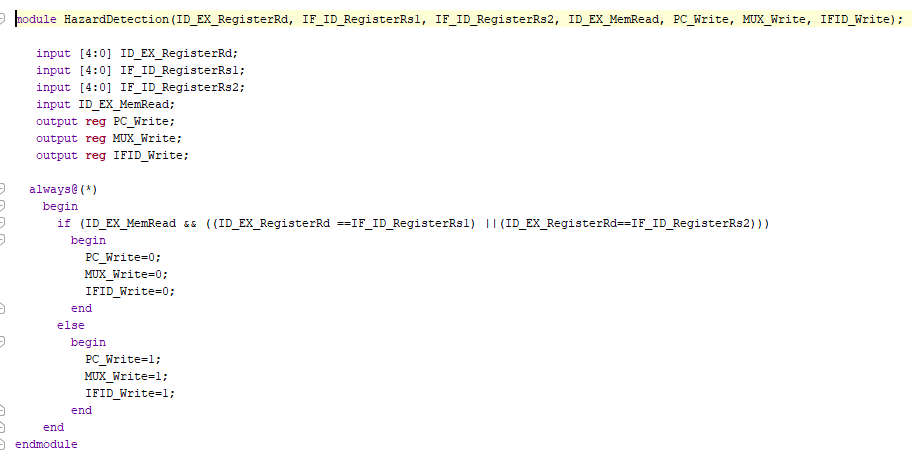
**Wave**

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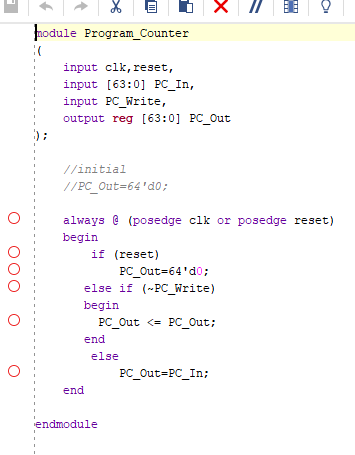
**Intermediate Modules**

**Forwarding Unit**

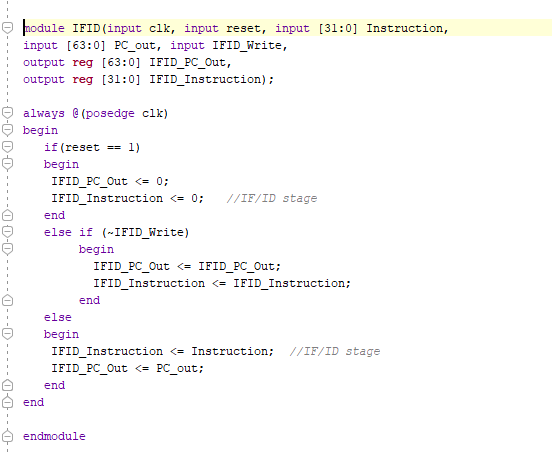
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**Hazard Detection (for Data Hazards)  
**

**Program Counter**

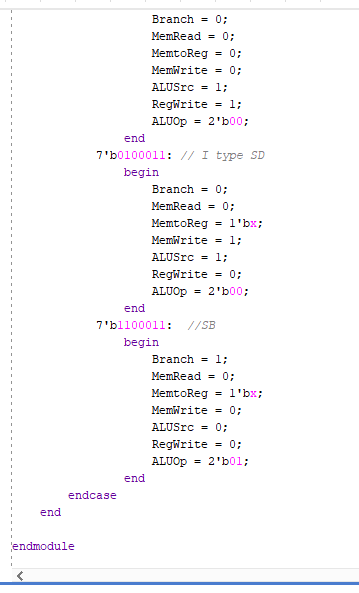
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**IFID Pipeline Register**

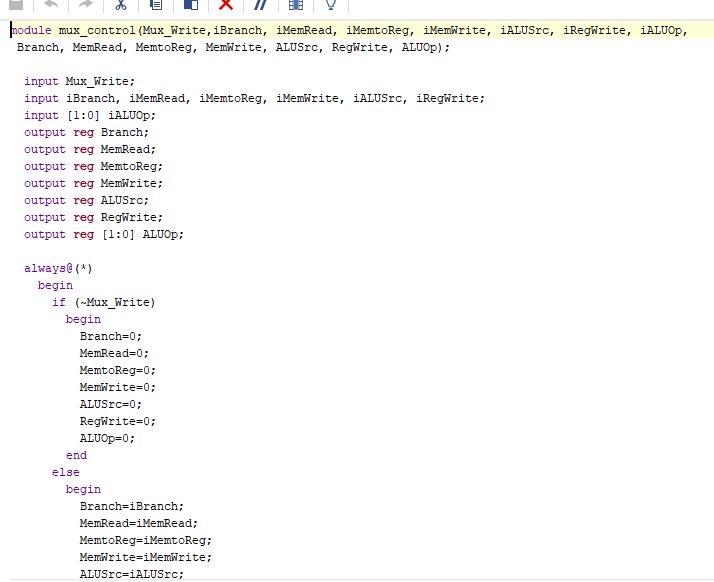
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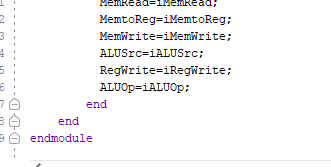
**Control Unit**

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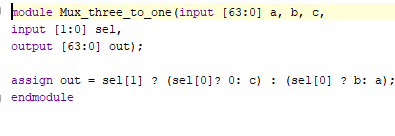
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**Mux Control unit**

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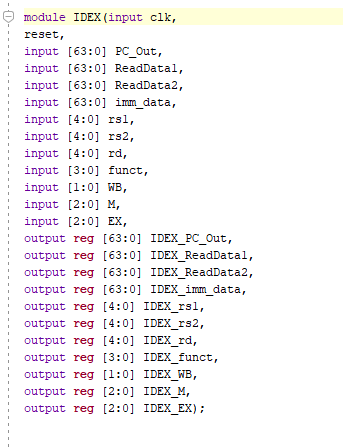
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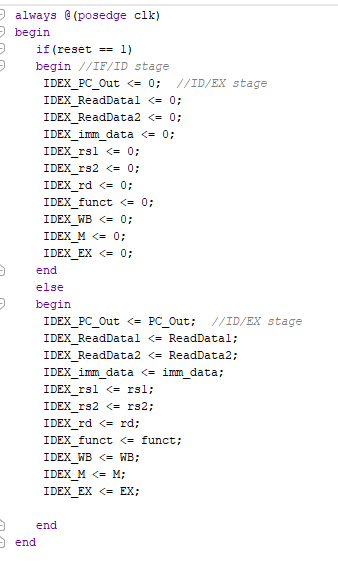
**3X1 Mux**

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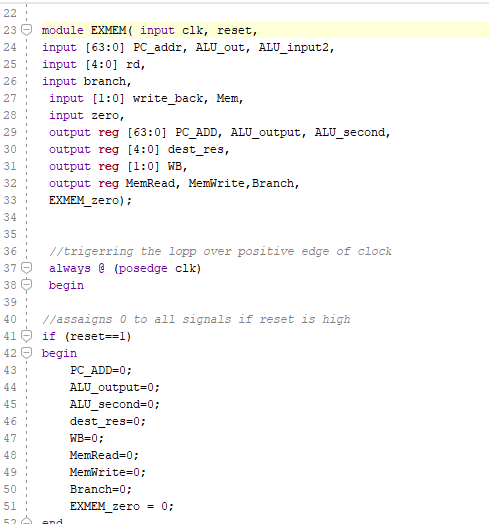
**Register File, Instruction Memor, ALu Control, Mux, ALu 64 bit, adder Instruction Parser,, Immidiate Genreator , Data Memory are all attached and commonly used by both versions**

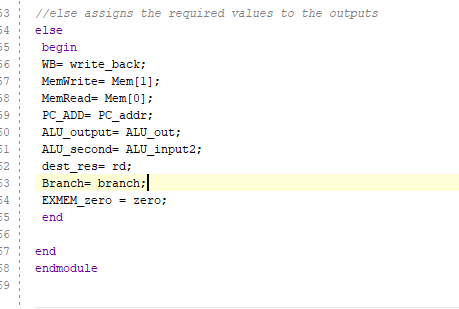
**IDEX Pipeline Register**

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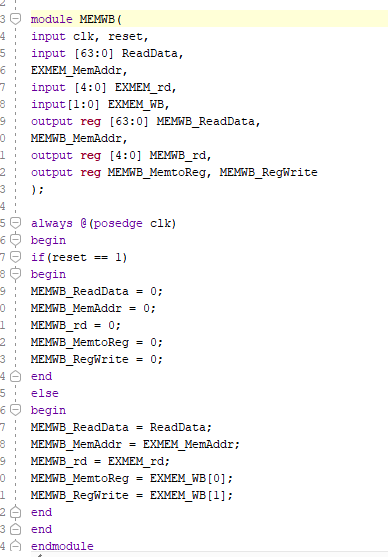
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**EXMEM Pipline Register**

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**MEMWB Pipeline Register**

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